Attorney's Docket No.: 10559-177001 / P8237

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kalpesh Mehta
Serial No.: 09/771,374
Filed: January 26, 2001
Title: APPORTIONING A SHARED COMPUTER RESOURCE

Art Unit: 2194
Examiner: Li Zhen

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Sir:

Pursuant to the 37 C.F.R. § 41.31, M.P.E.P. § 1207.04, and the Notice of Appeal filed herewith, Applicant hereby files this Brief on Appeal to supplement the Brief on Appeal filed June 27, 2005 and to respond to the new grounds for rejection raised in the Office Action mailed September 16, 2005.

(1) Real Party in Interest

The case is assigned of record to Intel Corp., who is hence believed to be the real party in interest.

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

December 15, 2005
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Julie H. Giordano
Signature

Julie H. Giordano
Typed or Printed Name of Person Signing Certificate

(2) Related Appeals and Interferences

There are no known related appeals and/or interferences.

(3) Status of Claims

Applicant incorporates by reference the status of claims included in the appeal brief filed June 27, 2005, which indicates:

Claims 4, 5, 9-10, 14-20 are pending and are rejected; and

Claims 1-3, 6-8 and 11-13 have been previously canceled.

(4) Status of Amendments

Applicant incorporates by reference the status of amendments included in the appeal brief filed June 27, 2005, which indicates:

An amendment after final was filed on January 20, 2005, and was indicated as being entered in an advisory action mailed April 5, 2005 (paper number 20050330).

No amendments have been filed since then.

(5) Summary of Claimed Subject Matter

Applicant incorporates by reference the summary of claimed subject matter included in the appeal brief filed June 27, 2005, which indicates:

Claim 18 defines a method which allows computer processes to be assigned with both an access value and a priority value. Each of the plurality of computer resources is assigned an access value (page 3 lines 26-27), and a priority value (page 4 lines 10-12). The priority value can be either high or low priority see page 4 lines 11-12. During a first access cycle, access is provided to processes first whose access value represents high priority and whose access value represents the access should still be granted. See generally page 4 lines 23-30. The access values may be reallocated after each cycle, see page 5 lines 15-17.

Claim 18 requires determining that all priority high requests have access values that indicate no additional access should be granted see page 5 lines 1-5. After that determining, access is provided to the low priority requests see page 5 line for-19. After both the high and low requests have been given access, a new cycle is started, see page 5 line 26 through page 6 line 2.

Claim 19 defines assigning an access value and a priority value (page 3 lines 26-27 and page 4 lines 10-12). Claim 19 defines that access during the first access cycle access is first provided to the high priority processes and the access value is adjusted, page 4 lines 23-30; page 5 lines 15-17.

Claim 19 defines providing access to the low priority requests after that, page 5 lines 4-19 and starting a new cycle after both high and low requests have been granted, see page 5 line 26 through page 6 line 2.

Claim 20 defines a controller with ports, including ports for connecting to different processes see generally page 3 lines 7-9. Claim 20 defines a memory 130, see page 3 line 9. The memory stores access values see page 3 lines 18-20. The controller operates to assign an access value and a priority value to the computer resources (page 3 lines 26-27 and page 4 lines 10-12) provides accesses to the high priority values first, (page 4 lines 23-30) reallocates those values (page 5 lines 15-17) after that provides access to the low priority requests (page 5 lines 4-19) and then starts a new cycle (page 5 line 26 through page 6 line 2).

(6) Grounds of Rejection

The additional ground of rejection for review on appeal is whether claims 4, 5, 9, 10 and 14-20 are properly rejected under 35 U.S.C. § 103 as being obvious over U.S. Patent No. 6,363,445 to Jeddeloh (hereinafter "Jeddeloh") in view of U.S. Patent No. 5,884,051 to Schaffer, et al. (hereinafter "Schaffer").

(7) Argument

The September 16th Office Action removes the rejection of claims 4, 5, 9, 10 and 14-20 as obvious over U.S. Patent No. 6,067,557 to Hedge in view of Schaffer. Instead, the September 16th Office Action rejects the same claims as obvious over Jeddeloh in view of Schaffer. Of these claims, claims 18, 19, and 20 are independent.

INDEPENDENT CLAIM 18

The rejection of claim 18 contends that it would have been obvious for one of ordinary skill to combine Jeddeloh and Schaffer to arrive at the claimed subject matter. Applicant respectfully disagrees.

In this regard, Jeddeloh relates to the arbitration of bandwidth on a bus. Each device on Jeddeloh's bus is assigned both a priority value and a weighted bandwidth. *See Jeddeloh*, col. 3, line 11-13. The priority value corresponds to the priority ranking of the device relative to the other devices on the bus, and the weighted bandwidth reflects, at least in part, the performance ability of the device. *See Jeddeloh*, col. 3, line 5-7. Faster devices are initially assigned a higher weighted bandwidth. *See Jeddeloh*, col. 4, line 13-19.

Jeddeloh monitors the bandwidth usage of each device to determine if each device's usage exceeds the expectations set forth in the weighted bandwidth. Jeddeloh also periodically changes the weighted bandwidths to reflect actual usage.

FIG. 3 of Jeddeloh illustrates these processes. In particular, bandwidth is initially allocated to a single, highest-priority device. *See, e.g., Jeddeloh*, FIG. 3, at 104. So long as its actual bandwidth consumption does not exceed the expectations set forth in the weighted bandwidth, bandwidth can continue to be allocated to this same highest-priority device. *See, e.g, Jeddeloh*, FIG. 3, "NO" branch from 112. However, when the actual bandwidth consumption exceeds the expectations set forth in the weighted bandwidth, the priority of the highest-priority device is set to the lowest possible value. *See, e.g, Jeddeloh*, FIG. 3, "YES" branch from 112. A high priority device that consumes its allocated bandwidth is thus transformed into the lowest-priority device, and low priority devices that have not consumed their allocated bandwidth are pushed into the ranks of the highest priority devices. Since this process repeats itself over and over, priority values for each device continuously change as each device moves into a high priority position, uses its allocated bandwidth, and is then relegated to the lowest-priority position.

Jeddeloh also describes that the expectations set forth in the weighted bandwidth must occasionally be changed. *See, e.g, Jeddeloh*, col. 5, line 22-29. Once again, FIG. 3 of Jeddeloh is illustrative. When bandwidth has been allocated a certain number of times (i.e., when the total number of allocations exceeds a "terminal value"), Jeddeloh's weighted bandwidths can be reset to reflect the actual consumption of bandwidth by the devices. *See, e.g, Jeddeloh*, FIG. 3, "YES" branch from 118.

Please note that the total number of allocations must be large, and the cycling of priority values for each device must occur a number of times, for a meaningful resetting of the weighted bandwidths to occur. For example, if weighted bandwidths are reset after only a few bandwidth allocations, then the number of measurements would be too small, the statistics uncertain, and devices would not be allocated bandwidth "in approximate proportion to a desired weighted bandwidth." Rather, the devices that, for short periods of time, consume bandwidth would receive excessive allocations. This directly contradicts Jeddeloh's recommendations. *See, e.g., Jeddeloh*, col. 3, line 1-10.

Schaffer describes that access to a bus can be allocated based on one of three priority levels (i.e., a "master dynamic priority level," an "arbiter dynamic priority level," or a

"programmable fixed priority level") that can override each other based on the state of Schaffer's machine. *See Schaffer*, col. 3, line 43-55.

I. Jeddeloh and Schaffer Neither Describe nor Suggest the Subject Matter of Claim 18.

Claim 18 indicates that it is to be determined that both high priority requests and low priority requests each have access values that represent no further access should be granted in a first access cycle before starting a new access cycle with new access values and priority values.

Neither Jeddeloh nor Schaffer describes or suggests such a determination. As discussed above, Jeddeloh's device generally operates continuously, relabeling highest priority devices as the lowest-priority devices as they consume bandwidth. Such a continuous operation does not determine that no further access should be granted in a first access cycle but rather that access is always to be granted to one device or another.

Even if one were to take Jeddeloh's occasionally resetting of the weighted bandwidth allocations to be "access cycles" (a contention which was not raised in the rejection), the subject matter of claim 18 would still not be achieved. Jeddeloh's access values never represent that no further access should be granted. Rather, a count of the total number of allocations

simply indicates that the weighted bandwidth allocations should be changed. Further, Jeddeloh does not describe new access values and priority values after the weighted bandwidth allocations have been reset. Rather, only weighted bandwidth allocations are changed.

Schaffer adds nothing to remedy this deficiency in Jeddeloh. Schaffer does not appear to determine that both high priority requests and low priority requests each have access values that represent no further access should be granted in a first access cycle, nor does Shaffer start a new access cycle with new access values and priority values. Indeed, the rejection does not contend otherwise.

Instead, the rejection points to Schaffer, col. 12, line 47-64 as allegedly showing "access cycles." Applicant respectfully disagrees. Attention is respectfully directed to FIG. 9, which shows that the cycles in the cited portion of Schaffer are clock cycles and not access cycles.

Since the claimed subject matter is neither described nor suggested by either Jeddeloh or Schaffer, a *prima facie* case of obviousness has not been established. Applicant therefore requests that the obviousness rejection of claim 18 and its dependent claims be withdrawn.

II. Jeddeloh Leads One of Ordinary Skill away from the Subject Matter of Claim 18.

Claim 18 recites that, during a first access cycle, it is to be determined that all high priority requests have access values that indicate that no additional access should be granted.

In contrast, Jeddeloh teaches that access is almost continuously granted to the highest priority devices. In Jeddeloh, when an individual high priority device consumes its bandwidth allocation, the priority of this device is set to zero and bandwidth is allocated to a new high priority device. Given this almost continuous change of the priorities of Jeddeloh's devices, Jeddeloh will grant access to the high priority devices almost continuously. In other words, there is never a determination in Jeddeloh that no additional access should be granted to all high priority devices—rather the priority of the devices is to change so that access is continuously granted to highest priority devices.

The rejection would have one of ordinary skill discard this express teaching of Jeddeloh. The rejection has set forth no reason why one of ordinary skill would do so, but rather has impermissibly used applicant's own disclosure as a guide for establishing what would be obvious to one of ordinary skill.

Accordingly, Applicant submits that any rejection that relies on Jeddeloh is improper and further requests that the rejection of claim 18 and its dependent claims be withdrawn.

INDEPENDENT CLAIMS 19 and 20

Claims 19 and 20 should be allowable for analogous reasons to those discussed above. In particular, Jeddeloh and Schaffer neither describe nor suggest determining that both high priority requests and low priority requests each have access values that represent no further access should be granted or starting a new access cycle with new access values and priority values.

Further, Jeddeloh describes that access is almost continuously granted to the highest priority devices, which would lead one of ordinary skill away from any determination that all high priority requests have access values that indicate that no additional access should be granted.

Since the claimed subject matter is neither described nor suggested by either Jeddeloh or Schaffer, a *prima facie* case of obviousness has not been established. Further, since Jeddeloh would lead one of ordinary skill away from the claimed subject matter, any rejection that relies on Jeddeloh is beleived to be improper. Applicant therefore requests that the obviousness rejections of claims 19, 20, and the claims dependent therefrom be withdrawn.

Each of the dependent claims should be allowable by virtue of their dependency, as well as on their own merits.

In view of the above, it is respectfully suggested that all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

No fee is believed due at this time. If this is in error, or charges are due for any reason, please apply such fees or charges to Deposit Account No. 06-1050.

Respectfully submitted,

Date: December 15, 2005

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Appendix of Claims

4. The method according to claim 18 wherein at least one of the computer processes is an isochronous process.

5. The method according to claim 18 wherein at least one of the computer processes is an asynchronous process.

9. The technique according to claim 19 wherein at least one of the computer processes is an isochronous process.

10. The technique according to claim 19 wherein at least one of the computer processes is an asynchronous process.

14. The apparatus according to claim 20 wherein at least one of the computer processes is an isochronous process.

15. The apparatus according to claim 20 wherein at least one of the computer processes is an asynchronous process.

16. The apparatus according to claim 20 wherein the controller device is a memory controller.

17. The apparatus according to claim 20 wherein the shared

memory resource is a shared memory bank.

18. A method, comprising:

assigning an access value and a priority value to each of a plurality of computer processes which request access to a shared computer resource, where the priority value can be high priority or low priority;

during an first access cycle, first providing access to processes whose access value represents high priority and whose access value represents that access should still be granted during the access cycle, and after granting each access, adjusting an access value associated with said each access, to indicate that additional access has been granted;

determining, during said first access cycle, that all high priority requests have access values that indicate that no additional access should be granted;

responsive to said determining, in said first access cycle, providing access to low priority requests whose access values represent that access should be granted, and adjusting access values after granting the access; and

after determining that both the high priority requests and low priority requests each have access values that represent no further access should be granted in said first access cycle,

starting a new access cycle with new access values and priority values.

19. An article comprising a computer readable media which stores executable instructions for controlling access to a shared computer resource by at least two computer processes, the instructions, when executed, causing the computer to:

assign an access value and a priority value to each of a plurality of computer processes which request access to a shared computer resource, where the priority value can be high priority or low priority;

during a first access cycle, first provide access to processes whose access value represents high priority and whose access value represents that access should still be granted during the access cycle, and after granting each access, adjust an access value associated with said access to indicate that additional access has been granted;

determine, during said first access cycle, that all high priority requests have access values that indicate that no additional access should be granted;

responsive to said determining, in said first access cycle, provide access to low priority requests whose access values indicate that access should be granted, and adjust access values

after granting the access; and

after determining that both the high priority requests and low priority requests each have access values that represent no further access should be granted in said first access cycle, start a new access cycle with new access values and priority values.

20. An apparatus, comprising:

a controller device, having a first port for connecting to a shared resource, and at least one second port for connecting to a plurality of different processes which are requesting access to the shared resource,

a memory operating to store access values,

said controller operating to:

assign an access value and a priority value to each of a plurality of computer processes which request access to a shared computer resource, where the priority value can be high priority or low priority, and store said values in said memory, during a first access cycle, first controlling said processes to provide access to processes whose access value represents high priority and whose access value represents that access should still be granted during the access cycle, and after granting each access, adjusting an access value associated with said

access to indicate that additional access has been granted, determining, during said first access cycle, that all high priority requests have access values that indicate that no additional access should be granted, responsive to said determining, in said first access cycle, providing access to low priority requests whose access values represent that access should be granted, and adjusting access values after granting the access; and

after determining that both the high priority requests and low priority requests each have access values that represent no further access should be granted in said first access cycle, starting a new access cycle with new access values and priority values.

(8) Appendix of Evidence

None.

(9) Appendix of Related Proceedings

None.